

U.S. Appln. No. 10/039,316
Reply to Office Action dated July 6, 2005

PATENT
450100-03548

REMARKS/ARGUMENTS

Reconsideration and withdrawal of the rejections of the application are respectfully requested in view of the amendments and remarks herewith. The present Amendment is being made to facilitate prosecution of the application.

I. STATUS OF THE CLAIMS AND FORMAL MATTERS

Claims 1, 3-6, 8-12, 14-17 and 19-23 are pending in this application. Claims 1, 6, 12, 17, and 23, which are independent, are hereby amended. Claims 2, 7, 13, 18, 24, and 25 have been canceled without prejudice or disclaimer of subject matter. It is submitted that these claims, as originally presented, were in full compliance with the requirements of 35 U.S.C. §112. Support for this amendment is provided throughout the Specification as originally filed. No new matter has been introduced by this amendment. Changes to claims are not made for the purpose of patentability within the meaning of 35 U.S.C. §101, §102, §103, or §112. Rather, these changes are made simply for clarification and to round out the scope of protection to which the Applicants are entitled.

II. REJECTIONS UNDER 35 U.S.C. §101

Claims 24 and 25, which were rejected under 35 U.S.C. §101, are hereby canceled, obviating the rejection.

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III. REJECTIONS UNDER 35 U.S.C. §103(a)

Claims 1-3, 6-8, 11-14, 17-19 and 22-25 were rejected under 35 U.S.C. §103(a) as allegedly unpatentable over U.S. Patent No. 5,805,799 to Fredrickson et al. in view of U.S. Patent No. 5,457,789 to Dietrich, et al.

Claims 4, 5, 9, 10, 15, 16, 20 and 21 were rejected under 35 U.S.C. §103(a) as allegedly unpatentable over U.S. Patent No. 5,805,799 to Fredrickson, et al. in view of U.S. Patent No. 5,457,789 to Dietrich, et al. and further in view of U.S. Patent No. 6,252,961 to Hogan.

Independent claim 1 recites, *inter alia*:

"...a memory interface unit for accessing said data storage means which has a data storage area consisting of a plurality of blocks, each of which consists of a plurality of sectors which have the actual data part and the redundant part in each of the sectors; and

a control unit for controlling said memory interface unit,

wherein said memory interface unit includes a cryptosystem unit that generates an integrity check value based on actual data to be stored in the actual data part in response to a data-writing command from said control unit to said data storage means, and stores said integrity check value in the redundant part of each of the sectors in said data storage means." (emphasis added)

Thus, one feature of the invention is that the memory interface unit "stores said integrity check value in the redundant part of each of the sector in said data storage means".

When data is read, the memory I/F unit 300 (shown in FIG. 2 of the Specification) executes ICV checking in units of sectors. If the memory I/F unit 300 has found invalid data which has interpolation, it does not transfer the data to the control unit 205. When data is written, the memory I/F unit 300 executes processing that calculates and writes, in the redundant part, the ICV of each sector." (See application publication [0401])

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This feature connects data parts by the file system of the device 200 when the ICV is stored in the redundant part can be performed. Accordingly, the file system of the device 200 may simply connect data parts, excluding redundant parts, so that ant additional processing does not need to be performed. (See application publication [0405])

As understood by Applicants, U.S. Patent No. 5,805,799 to Fredrickson et al. (hereinafter, merely "Fredrickson") relates to a data integrity code including logical block address ("LBA") and circuit implementation. The code and implementing circuitry are utilized to enable data block LBA verification during a block transfer and retrieval process. The data integrity code has embedded LBA information and also serves as a crosscheck code used to detect miscorrection by an error correction code ("ECC"). Data integrity/cross-check redundancy with LBA is appended to data blocks transmitted to a buffer memory and verified after the data block has been transferred from the buffer.

As understood by Applicants, U.S. Patent No. 5,457,789 to Dietrich, et al. (hereinafter, merely "Dietrich") relates to checking memory access by individual processing elements by a common controller. The controller includes a table of values defining valid memory locations for a task. The controller verifies the address value used by each instruction to ensure that it is within a valid memory area for the particular task.

Applicants submit that nothing has been found in Fredrickson or Dietrich, taken alone or in combination, that would disclose or suggest the above-identified features of claim 1. For example, Frederickson does not have the actual data part and the redundant part in sector. Moreover, Frederickson does not recode an integrity check value in the redundant part.

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Applicants submit that Fredrickson and Dietrich fail to disclose or suggest a memory interface unit for accessing said data storage means which has a data storage area consisting of a plurality of blocks, each of which consists of a plurality of sectors which have the actual data part and the redundant part in each of the sectors, as recited in claim 1. Furthermore, Applicants submit that neither Fredrickson or Dietrich teach or suggest a memory interface unit includes a cryptosystem unit that generates an integrity check value and stores said integrity check value in the redundant part of each of the sectors in said data storage means, as recited in claim 1. Therefore, Applicants submit that claim 1 is patentable.

Independent claims 6, 12, 17, and 23 are similar in scope and believed to be patentable for similar reasons.

IV. DEPENDENT CLAIMS

The other claims in this application are each dependent on a dependent claim discussed above, and are therefore believed patentable for at least the same reasons. Since each dependent claim is also deemed to define an additional aspect of the invention, however, the individual reconsideration of the patentability of each on its own merits is respectfully requested.

CONCLUSION

In the event the Examiner disagrees with any of statements appearing above with respect to the disclosures in the cited references, it is respectfully requested that the Examiner specifically indicate those portions of the reference, or references, providing the basis for a contrary view.

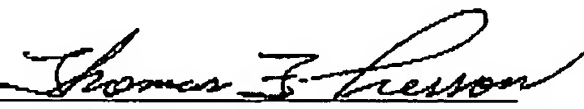
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Please charge any additional fees that may be needed, and credit any
overpayment, to our Deposit Account No. 50-0320.

Respectfully submitted,

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